IN THE CLAIMS:

Please amend claims 1, 4, 7, 10, 16, 19, and 22 and **add** new claims 23-25, as shown in the complete list of claims that is presented below.

1. (currently amended) A semiconductor package which has a surface with a plurality of connection terminals to be connected to wiring on a board and a plurality of test terminals that are electrically isolated from he wiring on ~~a joint surface thereof to~~ said board,

wherein ~~a first area where~~ said connection terminals are arranged in a first area at predetermined pitches in a lattice ~~and a second area where~~ said test terminals are arranged in a second area at pitches narrower than said predetermined pitches in a lattice ~~are placed~~.

2. (original) The semiconductor package according to claim 1, wherein said connection terminals and said test terminals are formed by solder balls..

3. (original) The semiconductor package according to claim 1, wherein said connection terminals and said test terminals are formed by lands.

4. (currently amended) The semiconductor package according to claim 1, wherein said second area is placed in the center of said ~~joint~~ surface, and said first area is placed in the periphery of said ~~joint~~ surface so as to surround said second area.

5. (original) The semiconductor package according to claim 4, wherein said connection terminals and said test terminals are formed by solder balls.

6. (original) The semiconductor package according to claim 4, wherein said connection terminals and said test terminals are formed by lands.

7. (currently amended) The semiconductor package according to claim 1, wherein said second area is placed in the periphery of said ~~joint~~ surface, and said first area is placed so as to surround said second area.

8. (original) The semiconductor package according to claim 7, wherein said connection terminals and said test terminals are formed by solder balls.

9. (original) The semiconductor package according to claim 7, wherein said connection terminals and said test terminals are formed by lands.

10. (currently amended) The semiconductor package according to claim 7, wherein said second area is placed ~~on layout of~~ where a high-heat-buildup circuit ~~mounted~~ disposed.

11. (original) The semiconductor package according to claim 10, wherein said connection terminals and said test terminals are formed by solder balls.

12. (original) The semiconductor package according to claim 10, wherein said connection terminals and said test terminals are formed by lands.

13. (original) The semiconductor package according to claim 1, wherein said first area is formed in a plurality of places, and said second area is placed so as to isolate said first areas respectively formed in said plurality of places from each other.

14. (original) The semiconductor package according to claim 13, wherein said connection terminals and said test terminals are formed by solder balls.

15. (original) he semiconductor package according to claim 13, wherein said connection terminals and said test terminals are formed by lands.

16. (currently amended) ~~The~~ A semiconductor package ~~according to claim 13, wherein the test terminals in said second area are mounted on ground.~~ which has a surface with a

plurality of connection terminals to be connected to wiring on a board and a plurality of test terminals for testing circuitry within the package before the connection terminals are connected to the wiring on the board and to be connected to a ground on the board when the connection terminals are connected to the wiring on the board,

wherein said connection terminals are arranged in a first area at predetermined pitches in a lattice and said test terminals are arranged in a second area at pitches narrower than said predetermined pitches in a lattice.

17. (original) The semiconductor package according to claim 16, wherein said connection terminals and said test terminals are formed by solder balls.

18. (original) The semiconductor package according to claim 16, wherein said connection terminals and said test terminals are formed by lands.

19. (currently amended) The semiconductor package according to claim 1, wherein said surface is rectangular and said second area is placed in the four corners of said ~~joint~~ rectangular surface, and said first area is placed in an area except for said four corners.

20. (original) The semiconductor package according to claim 19, wherein said connection terminals and said test terminals are formed by solder balls.

21. (original) The semiconductor package according to claim 19, wherein said connection terminals and said test terminals are formed by lands.

22. (currently amended) A lead-type semiconductor package which has a plurality of connection leads to be connected to wiring on a board and a plurality of test leads that are electrically isolated from the wiring on said board,

wherein said connection leads are arranged at predetermined pitches, and said test leads are arranged at pitches narrower than said predetermined pitches.

23. (new) A semiconductor device having the semiconductor package of claim 1, in combination with the board and mounted on the board.

24. (new) A semiconductor device having the semiconductor package of claim 16, in combination with the board and mounted on the board.

25. (new) A semiconductor device having the semiconductor package of claim 22, in combination with the board and mounted on the board.